

What Is Claimed Is:

- 1 1. A method forming junction isolation to isolate active
2 elements, comprising the steps of:
3 providing a semiconductor substrate having a plurality of
4 active areas and at least one isolation area between
5 any two active areas;
6 forming a first gate structure on part of the substrate
7 located in the active areas and a second gate structure
8 on the substrate located in the isolation area;
9 forming a first doped region in the substrate located at two
10 sides of the first gate structure and two sides of the
11 second gate structure;
12 forming a bottom anti-reflection layer on the substrate, the
13 first gate structure and the second gate structure;
14 anisotropic etching back part of the bottom anti-reflection
15 layer to expose the second gate structure;
16 removing the second gate structure to expose the surface of
17 the substrate;
18 forming a second doped region in the substrate located in
19 the isolation area, wherein a type of dopant in the
20 first doped region is opposite to that in the second
21 doped region; and
22 removing the bottom anti-reflection layer.

1 2. The method according to claim 1, wherein the first gate
2 structure and the second gate structure are simultaneously formed
3 on the substrate.

1 3. The method according to claim 1, wherein the second
2 gate structure serves as a dummy gate structure.

1 4. The method according to claim 2, wherein the method of
2 forming the first gate structure and the second gate structure
3 comprises the steps of:

4 forming an insulation layer on the substrate;
5 forming a conductive layer on the insulation layer; and
6 anisotropic etching back part of the conductive layer and
7 the insulation layer to form a gate layer and a gate
8 insulation layer on the substrate.

1 5. The method according to claim 4, wherein the insulation
2 layer is a SiO_2 layer.

1 6. The method according to claim 4, wherein the conductive
2 layer is a polysilicon layer.

1 7. The method according to claim 1, wherein the first
2 doped region is implanted with N-type ions and the second doped
3 region is implanted with P-type ions.

1 8. The method according to claim 1, wherein the first
2 doped region is implanted with P-type ions and the second doped
3 region is implanted with N-type ions.

1 9. The method according to claim 1, wherein the
2 anti-reflection layer is an organic layer.

1 10. A method of forming junction isolation to isolate
2 active elements, comprising the steps of:

3 providing a semiconductor substrate having a plurality of
4 active areas and at least one isolation area between
5 any two active areas;
6 forming a first gate structure on part of the substrate
7 located in the active areas and a second gate structure
8 on the substrate located in the isolation area;
9 forming a first doped region in the substrate located at two
10 sides of the first gate structure and two sides of the
11 second gate structure;
12 forming a bottom anti-reflection layer on the substrate, the
13 first gate structure and the second gate structure;
14 forming a patterned photoresist layer on the bottom
15 anti-reflection layer located in the active areas;
16 using the patterned photoresist layer as a mask, anisotropic
17 etching back part of the bottom anti-reflection layer
18 to expose the second gate structure;
19 removing the second gate structure to expose the surface of
20 the substrate;
21 forming a second doped region in the substrate located in
22 the isolation area, wherein a type of dopant in the
23 first doped region is opposite to that in the second
24 doped region;
25 removing the patterned photoresist layer; and
26 removing the bottom anti-reflection layer.

1 11. The method according to claim 10, wherein the first
2 gate structure and the second gate structure are simultaneously
3 formed on the substrate.

1 12. The method according to claim 10, wherein the second
2 gate structure serves as a dummy gate structure.

1 13. The method according to claim 11, wherein the method
2 of forming the first gate structure and the second gate structure
3 comprises the steps of:

4 forming an insulation layer on the substrate;
5 forming a conductive layer on the insulation layer; and
6 anisotropic etching back part of the conductive layer and
7 the insulation layer to form a gate layer and a gate
8 insulation layer on the substrate.

1 14. The method according to claim 13, wherein the
2 insulation layer is a SiO₂ layer.

1 15. The method according to claim 13, wherein the
2 conductive layer is a polysilicon layer.

1 16. The method according to claim 10, wherein the first
2 doped region is implanted with N-type ions and the second doped
3 region is implanted with P-type ions.

1 17. The method according to claim 10, wherein the first
2 doped region is implanted with P-type ions and the second doped
3 region is implanted with N-type ions.

1 18. The method according to claim 10, wherein the
2 anti-reflection layer is an organic layer.